SIGNAL PROCESSING AT 4.5 GBIT/S WITH SI-ICs FOR OPTICAL TRANSMISSION SYSTEMS

Gerhard Hanke

Research Institute of Deutsche Bundespost
Darmstadt, FRG

ABSTRACT

In the trunk network of Deutsche Bundespost optical transmission systems working at 2.4 Gbit/s will be implemented in the near future. This bitrate can be processed with commercial monolithic integrated GaAs-circuits. For higher bitrates, such as 4.5 Gbit/s, monolithic integrated Si-ICs must be used at the time being. In this paper it is shown that with only a few different types of ICs all the components for a transmission system can be built up using a sophisticated circuitry.

TRANSMISSION SYSTEM

The transmission system to be described here is an experimental one with which the optical components like laser diodes, photo diodes, and single mode fibers and also the electronic circuitry shall be tested at a bitrate of 4.519 Gbit/s. Furthermore it is used to demonstrate the quality of a high-rated system and to get experiences for a later commercial use. Therefore the bitrate of 4.519 Gbit/s has been chosen independently of any existing standard.

Optical Components

One problem of optical transmission systems is the poor receiver sensitivity of optical direct detection receivers. Therefore high bitrate systems should operate in the 1550 nm region, where the fiber attenuation is at minimum. To overcome dispersion problems single frequency lasers have to be used.

In our transmission system we use standard monomode fibers for the transmission line. These fibers have a minimum attenuation of .22 dB/km and a dispersion of 15 ps/(nm.km). The laser diode is a 1550 nm DFB laser with a mushroom structure and due to the very low parasitic capacitance it is well suited for high bitrates. Additionally, chirp effects are small so that dispersion penalty due to the high dispersion value of the standard monomode fiber can be accepted. For the optical receiver ternary APDs are used. At the bitrate of 4.5 Gbit/s a sensitivity of -25 dBm is achievable. With the maximum regenerator spacing of 36 km in the network of Deutsche Bundespost, a transmitter output power of 0 dBm is sufficient to span this distance at 4.5 Gbit/s.

Transmitter

The main task of the electronic part is to make the high bitrate available for testing, but furthermore it should be possible to insert it into the existing network. Therefore the basic bitrate is 141.248 Mbit/s which e.g. can be one digital TV-channel. Fig. 1 shows the block diagram of the system. Three groups of eight 141 Mbit/s channels are combined in three multiplexers into three parallel and clock-synchronous data streams of 1.129 Gbit/s each. By means of a 3B/4B line encoder they are converted into four signals of the same bitrate which then are multiplexed into the 4.519 Gbit/s output signal. This type of line encoding has been taken because of its rather simple circuitry, its good property with regard to clock recovery and reducing the number of required 141 Mbit/s channels. Because of the construction of the fast multiplexer, the master-clock needs only to have half the frequency of the output bitrate. For NRZ/RZ converting of the output signal a passive frequency doubler can be used in case of need.

One or more of the input channels can be controlled by pseudo-random sequences, which are used to measure the bit error rate of whole the system.

Receiver

The photo-diode is connected to the end of the fiber and followed by a transimpedance amplifier with MESFETs. A single-chip broadband limiting amplifier controlls the amplitude and phase regenerator which also acts as a first 1:2 demultiplexer. Two second demultiplexers produce the four 1.129 Gbit/s input sig-

0149-645X/88/0000-0853$01.00 © 1988 IEEE

nals for the 3B/4B-decoder. At the decoder output the original three 1.129 Gbit/s channels can be obtained. Synchronizing of these three signals is done by means of the decoding law. Each of the three last demultiplexers converts one 1.129 Gbit/s bitstream into eight 141 Mbit/s streams. Here synchronization is done by one specific 141 Mbit/s channel of the master demultiplexer.

As at the transmitting side the regenerator only needs half the bit repetition frequency as clock. The clock is extracted out of the NRZ data signal via a passive circuit using a dielectric resonator as filter.

INTEGRATED SI-CHIPS

Commercially available monolithic integrated GaAs-ICs have been used for bitrates up to 2.4 Gbit/s which at the moment seems to be the highest bitrate to be handled by these circuits (Ref. 1). To reach the 4.5 Gbit/s we therefore in addition are using monolithic integrated Si-ICs, which have been developed and fabricated by Ruhr-Universität Bochum and Siemens Munich (Ref. 2). The used technology is a standard ECL one with 2 um dimensions. The circuits partly reach bitrates up to 7 Gbit/s due to a careful optimization of all components, low internal switching levels and differential signal processing. A new generation of these circuits shall be produced with .8 um dimensions and will increase the available bitrate to more than 10 Gbit/s.

Multiplexer

The principle of the 4:1 multiplexer chip is shown in Fig. 2. Multiplexing is done in two steps: the four input signals first are combined into two streams of 2.259 Gbit/s each and after that in the last submultiplexer brought to the output bitrate (Ref. 3). The three submultiplexers consist only of gate-circuits which are clocked by an internal master-slave flip flop. The clock signal of 2.259 GHz is fed to the circuit in differential mode which results in 4 clock inputs because the last submultiplexer needs a time-delayed clock. The differential output signal is buffered inside the chip. The circuit has the following characteristics:

Maximum bit rate	6 Gbit/s
Switching times (20 to 80 %)	70 ps
Data inputs (single ended)	ECL
Clock inputs (differential)	400 mV
Data output (differential)	900 mV
Supply voltage	-5 V
Power consumption	575 mW

Limiting amplifier

The output signal of the transimpedance amplifier has an amplitude of about 5 mVpp, which must be amplified to the regenerator input voltage of 400 mVpp. This amplification is done by a broadband limiting amplifier, which has been optimized not for maximum bandwidth but for an optimal pulse response (Ref. 4). The principle of this 5-stage amplifier is shown in Fig. 3. The input emitter follower controls three equal amplifier units. These four stages are fed back in order to get an automatic offset control, for which the only external component, a 10 nF capacitor, is needed. A buffer follows as output stage. Technical data of this circuit are:

Maximum bitrate	>4 Gbit/s
Max. voltage gain (diff.)	54 dB
Input voltage range	1-400 mVpp
Dynamic range	52 dB
Const. output voltage swing	400 mVpp
Supply voltage	-5 V
Power consumption	350 mW

Regenerator and Demux

This chip, which is shown in Fig. 4, acts both, as a regenerator and a 1:2 demultiplexer (Ref. 5). All signals are in differential mode. The amplitude and phase regeneration is done by alternately switching the master slave flip flops with a clock signal having half the frequency of the input data, so e.g. the upper flip flop stores the 1st, 3rd, 5th etc., the lower stores the 2nd, 4th, 6th etc. bit of the input data stream. Synchronizing of this circuit therefore can be done very simply by inverting the clock signal. Data of the IC are:

Maximum bitrate	>4 Gbit/s
Input sensitivity (4 Gbit/s)	150 mVpp
Switching times (20 to 80%)	85 ps
Phase range (4 Gbit/s)	120 deg
Data output (differential)	800 mVpp
Supply voltage	-5 V
Power consumption	600 mW

Other Si-chips

In addition to the above described circuits some other chips are used: an Exclusive-OR-gate, working up to 2.7 Gbit/s, a single D-flip flop (>4 Gbit/s), a 1:8 ripple frequency divider (>7 GHz, Ref. 6) and a 2:1 multiplexer, which also can be used as an Exclusive-OR-gate (>4 Gbit/s). The improved circuits with .8 um dimensions will be available in Spring 1988.

ASSEMBLY

If bitrates exceed some Gbit/s the design of layout, interconnections, mounting and packaging has to be done under microwave-like conditions. But in contrast to classical microwave circuits, which normally are rather smallband ones, Gbit/s-circuits need the frequency range from DC to their upper limit. To produce e.g. at 4.5 Gbit/s a fairly rectangular appearing puls train, at minimum the third harmonic must be included, so that the circuit needs an upper frequency limit of 15 GHz. Therefore all signal interconnections can only be realized as carefully matched microstrip- or coaxial-lines, even for short distances. Because of the same reason high bitrate circuits normally should be used in dice form. But this leeds, on the other hand, to space problems due to the requirement for placing the matching resistors as close as possible around the chip. Additionally every resistor needs its connection to the ground-layer on the rear side of the substrate, which means a lot of metallized through-holes. The best solution of this problem would be on-chip matching resistors, which, if necessary, should be erasable.

For bitrates of more than about 2 Gbit/s thickfilm ceramic circuits have been found to be suitable for both, encapsulated and unencapsulated circuits. For bitrates of more than 5 or 6 Gbit/s thinfilm circuits should be preferred. Another possibility are copper-plated ceramic-filled Teflon substrates. The disadvantages of this material are poor mechanical and thermal properties and the missing possibility of integrated resistors and capacitors.

For this 4.5 Gbit/s-system all GaAs-devices have been mounted either on Teflon-substrates or, like the Si-chips, on ceramic thickfilm-circuits. These ceramic substrates also act as good heat sinks for the considerable power dissipation. All interconnection lines and resistors on the mounting side are screen-printed as well as the large areas of decoupling capacitors and power supply layers on the rear. Each Teflon- or thickfilm-circuit is a self contained device. Several devices are mounted on an etched printed circuit board and connected by means of 50 Ohm microstriplines or coaxial plugs. The fastest components, such as the 4:1-multiplexer, the limiting amplifier or the regenerating demultiplexer are built into microwave packages in order to avoid reflections at the transitions between striplines and coaxial lines.

CONCLUSION

By multiplexing 24 synchronous input channels of 141.248 Mbit/s each and 3B/4B line encoding an experimental optical transmission system with a bitrate of 4.519 Gbit/s has been developed. Hybrid thickfilm circuits and microwave suited layouts are the necessary requirements for it. As well GaAs-ICs as Si-ICs have been used in order to reach this bitrate at which the Si-ICs are taken for the highest bitrate.

ACKNOWLEDGEMENTS

The author wishes to thank Prof. Bosch, Prof. Rein and Prof. Langmann from Ruhr-Universität Bochum for making the fast multiplexer and regenerator chips available to him and he also wishes to thank Mr. Gohm from ANT/Backnang for the limiting amplifier and Dr. Treitinger from Siemens/Munich for multiplexer and divider chips.

REFERENCES

1. G. Hanke and B. Hein
   Monomode transmission system operating with 1300 nm lasers and 1550 nm DFB lasers at a bitrate of 2.23 Gbit/s
   Proceedings of ICC 1987, Seattle, WA, USA, pp. 6.3.1 - 6.3.5

2. G. Hanke
   Transmitter and receiver for an experimental 4.5 Gbit/s monomode fiber transmission system
   Proceedings of Globecom 1987, Tokyo, pp. 22.5.1 - 22.5.5

3. R. Reimann and H.-M. Rein
   A 4:1 time division multiplexer IC for bitrates up to 6 Gbit/s based on a standard bipolar technology
   IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, Oct.86, pp.785-789

4. R. Reimann and H.-M. Rein
   A 4 Gbit/s high-gain limiting amplifier for optical fiber receivers fabricated with a standard bipolar IC technology
   Proceedings of ISSCC 1987

5. D. Clawin e.a.
   Monolithisch integrierte Si-Bipolarschaltung mit Entscheider- und Demultiplexerfunktion für Bitraten bis 4 Gbit/s
   NTG-Fachberichte 96, 1986, S.273-278

6. P. Weger e.a.
   Static 7GHz frequency divider IC based on a 2 um Si bipolar technology
   Electronics Letters, Vol. 23, No. 5, Feb. 87, pp. 192-193

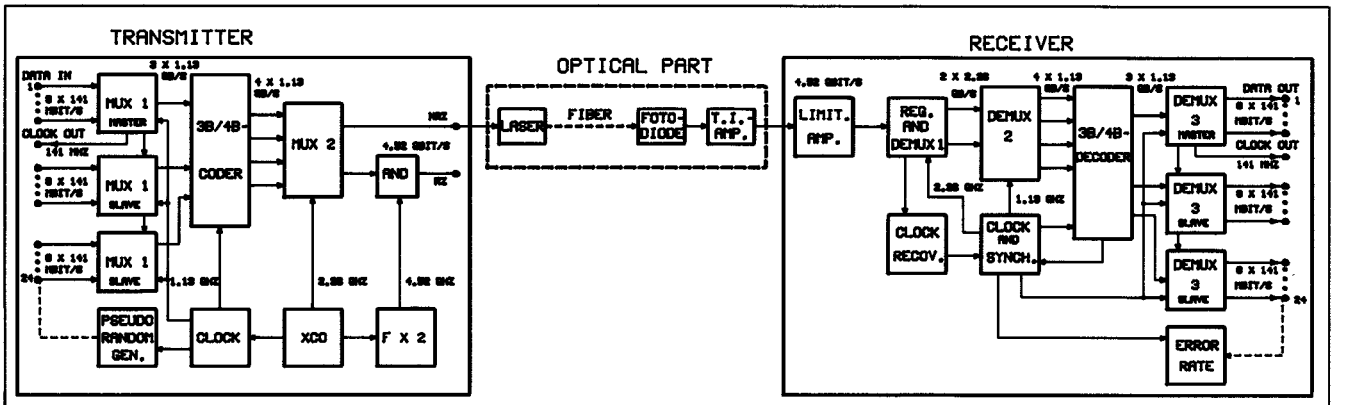

FIG. 1 BLOCK DIAGRAM OF THE TRANSMISSION SYSTEM

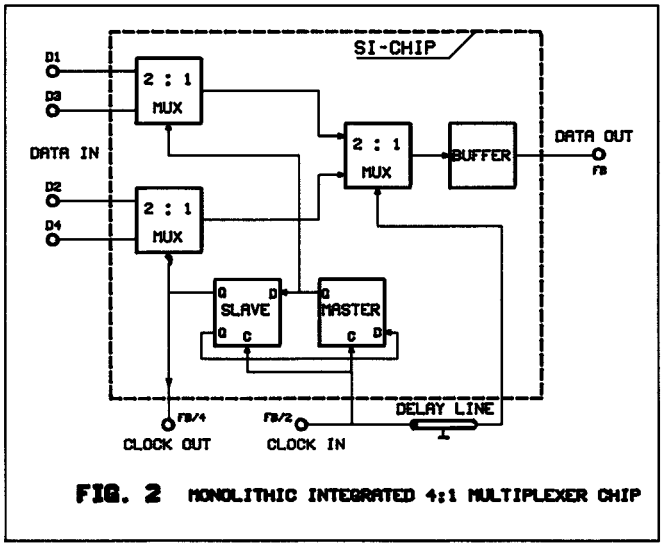

FIG. 2 MONOLITHIC INTEGRATED 4:1 MULTIPLEXER CHIP

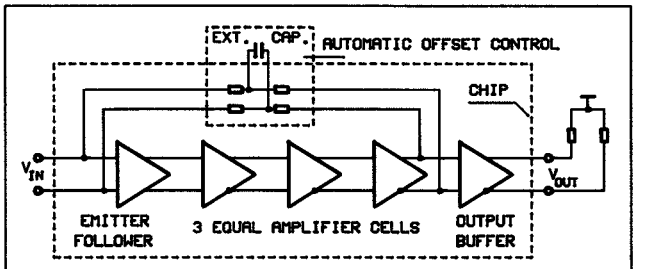

FIG. 3 BROADBAND LIMITING AMPLIFIER

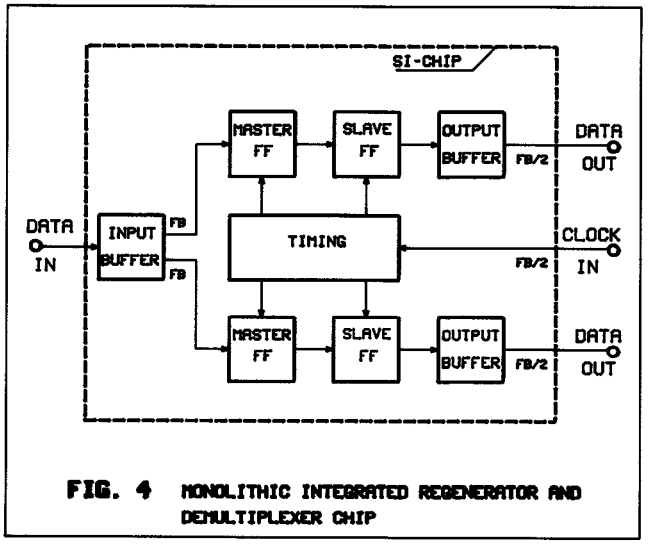

FIG. 4 MONOLITHIC INTEGRATED REGENERATOR AND DEMULTIPLEXER CHIP

Mailing Address

Gerhard Hanke
FI 42a
Forschungsinstitut der DBP
P.O.B. 5000
D-6100 DARMSTADT
FRG